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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/736,883	12/14/2000	Richard L. Solomon	00-450	7611

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EXAMINER	
VU, TRISHA U	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 09/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/736,883	SOLOMON ET AL.	
	Examiner	Art Unit	
	Trisha U. Vu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). ____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-9 and 11-30 are presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6, 8-9, and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bell (6,266,778) (herein after Bell) in view of Bell (6,170,030) (hereinafter Bell (6,170,030)).

As to claim 1, Bell teaches an interface system (bridges 805 and 810) suitable for coupling a first bus interface controller (Interface 834) with a second bus interface controller (interface 882) (Fig. 8), comprising: a first bus interface controller (Interface 834) and a second bus interface controller (interface 882) wherein the second bus interface controller is coupled to the first bus interface controller via an including: a command queuing interface (queues 824, 828 and/or queues 852, 854 and associate circuitry) including a path suitable for enqueuing a transaction; a command completion interface (queues 824, 828 and/or queues 852, 854 and associate circuitry) including a path suitable for reporting transaction completion (Fig. 8 and col. 13, lines 53-64); and a data transfer interface (queues 826, 830 and/or queues 856, 858 and associate circuitry)

suitable for transferring data (Fig. 8), wherein commands in the command queue include memory, input/output, configuration, and split completion commands (Fig. 8 and col. 7, lines 24-30, col. 14, lines 64-67, col. 15, lines 17-29), wherein the command queuing interface and the command completion interface are decoupled from the data transfer interface (Fig. 8). However, Bell does not explicitly disclose the command queuing interface including a first path and the command completion interface including a second path. Bell (6,170,030) teaches separate command queue (request queues 39 and/or 41) including a first path and command completion queue (DRC queues 43 and/or 45) including a second path (Fig. 2 and col. 6 line 19 to col. 7 line 31). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement separate command queue including a first path and command completion queue including a second path as taught by Bell (6,170,030) in the system of Bell to allow the command queue and the completion queue to operate in parallel fashion (col. 7 lines 1-53) and thus improve the system's speed.

As to claim 9, Bell teaches a method of transferring data, comprising: enqueuing a transaction on a command queuing interface (queues 824, 828 and/or queues 852, 854 and associate circuitry); transferring data corresponding to the transaction on a data transfer interface (queues 826, 830 and/or queues 856, 858 and associate circuitry) (Fig. 8); and receiving notification of completion of the transfer of data corresponding to the transaction, the notification reported on a command completion interface (queues 824, 828 and/or queues 852, 854 and associate circuitry) (Fig. 8), wherein a plurality of transactions are queued, wherein the transactions are completed without regard to an

order the transactions are queued (transactions and completions do not always get retired in the same order that they entered the transaction queues) (col. 13, lines 53-64 and col. 11, lines 1-5). However, Bell does not explicitly disclose the command queuing interface including a first path and the command completion interface including a second path. Bell (6,170,030) teaches separate command queue including a first path (request queues 39 and/or 41) and command completion queue including a second path (DRC queues 43 and/or 45) (Fig. 2 and col. 6 line 19 to col. 7 line 31). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement separate command queue including a first path and command completion queue including a second path as taught by Bell (6,170,030) in the system of Bell to allow the command queue and the completion queue to operate in parallel fashion (col. 7 lines 1-53) and thus improve the system's speed.

As to claims 2, 11, Bell further teaches command and control information are suitable for being exchanged on at least one of the command queuing interface and command completion interface while data is exchanged on the data transfer interface (col. 13, lines 53-64).

As to claims 3, 12, Bell further teaches data for transaction is suitable for being moved without respect to a current transaction being requested on a control bus (col. 13, lines 53-64).

As to claims 4, 13, Bell further teaches a backend master device (Processor 803) enqueues a transaction on the command queuing interface, at least one transfer of data is accomplished corresponding to the transaction queued on the command queuing

interface, and completion status of the transaction is reported on the command completion interface (Fig. 8 and col. 9, lines 66-67, col. 10, lines 1-27).

As to claim 5, Bell further teaches a plurality of transactions are queued, the transactions are completed without regard to an order the transactions are queued (col. 13, lines 53-64 and col. 11, lines 1-5).

As to claim 6, Bell further teaches the first bus interface controller is suitable for coupling to a backend device (Processor 803) and the second bus interface controller is suitable for coupling to an internal bus (PCI bus 820) of an information handling system (Fig. 8)

As to claim 8, Bell further teaches a plurality of data transfers on the data transfer interface are executed, the plurality of data transfers corresponding to a transaction queued on the command queuing interface (col. 9, lines 66-67 and col. 10, lines 1-27).

3. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bell (6,266,778) (herein after Bell) in view of Bell (6,170,030) (hereinafter Bell (6,170,030)) and further in view of Olarig et al. (6,449,677) (hereinafter Olarig).

As to claim 7, the argument for claim 1 above applies. Bell further teaches the second bus interface conforms to at least one of a PCI standard and PCI-X standard (PCI bus 820) (Fig. 8). However, Bell and Bell (6,170,030) do not explicitly disclose the first bus interface controller conforms to at least one of a USB standard, SCSI standard, fiber standard. Olarig teaches bus interface which conforms to SCSI bus standard (bus 111) (Fig. 1). It would have been obvious to one of ordinary skill in the art at the time the

invention was made to include SCSI standard as taught by Olarig in the system of Bell and Bell (6,170,030) because SCSI interfaces provide for faster data transmission rates (up to 80 megabytes per second) than standard serial and parallel ports.

4. Claims 14-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bell (6,266,778) (herein after Bell) in view of Bell (6,170,030) (hereinafter Bell (6,170,030)) and further in view of Kotha et al. (6,067,071) (hereinafter Kotha).

As to claim 14, Bell teaches an interface system (bridges 805 and 810) suitable for coupling a first bus interface controller (Interface 834) with a second bus interface controller (interface 882) (Fig. 8), comprising: a first bus interface controller (Interface 834) suitable for coupling to a backend device (Processor 803) and a second bus interface controller (interface 882) suitable for coupling to an internal bus (PCI bus 820) of and information handling system (Fig. 8), wherein the second bus interface controller is coupled to the first bus interface controller via an including: a command queuing interface (queues 824, 828 and/or queues 852, 854 and associate circuitry) suitable for enqueuing a transaction; a command completion interface (queues 824, 828 and/or queues 852, 854 and associated circuitry) suitable for reporting transaction completion (Fig. 8 and col. 13, lines 53-64); and a data transfer interface (queues 826, 830 and/or queues 856, 858 and associate circuitry) suitable for transferring data, wherein the command queuing interface and the command completion interface are decoupled from the data transfer interface (Fig. 8). However, Bell does not explicitly disclose the command queuing interface including a first path and the command completion interface

including a second path. Bell (6,170,030) teaches separate command including a first path queue (request queues 39 and/or 41) and command completion queue including a second path (DRC queues 43 and/or 45) (Fig. 2 and col. 6 line 19 to col. 7 line 31). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement separate command queue including a first path and command completion queue including a second path as taught by Bell (6,170,030) in the system of Bell to allow the command queue and the completion queue to operate in parallel fashion (col. 7 lines 1-53) and thus improve the system's speed. However, Bell does not explicitly disclose the first and second bus interface controllers are cores. Kotha teaches core logic (chipset) (col. 1, lines 14-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the first and second bus interface controllers to be cores (integrated into a chipset) as taught by Kotha in the system of Bell and Bell (6,170,030) to allow the circuit's functionality to be placed in smaller, lighter packages.

As to claim 15, Bell further teaches command and control information are suitable for being exchanged on at least one of the command queuing interface and command completion interface while data is exchanged on the data transfer interface (col. 13, lines 53-64).

As to claim 16, Bell further teaches data for transaction is suitable for being moved without respect to a current transaction being requested on a control bus (col. 13, lines 53-64).

As to claim 17, Bell further teaches a backend master device (Processor 803) enqueues a transaction on the command queuing interface, at least one transfer of data is accomplished corresponding to the transaction queued on the command queuing interface, and completion status of the transaction is reported on the command completion interface (Fig. 8 and col. 9, lines 66-67, col. 10, lines 1-27).

As to claim 18, Bell further teaches a plurality of transactions are queued, the transactions are completed without regard to an order the transactions are queued (col. 13, lines 53-64 and col. 11, lines 1-5).

As to claim 20, Bell further teaches a plurality of data transfers on the data transfer interface are executed, the plurality of data transfers corresponding to a transaction queued on the command queuing interface (col. 9, lines 66-67 and col. 10, lines 1-27).

5. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bell (6,266,778) (herein after Bell) in view of Bell (6,170,030) (hereinafter Bell (6,170,030)) and Kotha et al. (6,067,071) (hereinafter Kotha), and further in view of Cepulis et al. (6,061,754) (hereinafter Cepulis).

As to claim 19, the argument above for claim 14 applies. Bell further teaches the second bus interface conforms to at least one of a PCI standard and PCI-X standard (PCI bus 820). However, Bell and Kotha do not explicitly disclose the first bus interface controller is a triple bus interface that conforms to a USB standard, an SCSI standard, and a fiber standard. Cepulis teaches bus bridge/switch interfaces conforming to a USB

standard, a SCSI standard, and a fiber standard (co. 8, lines 64-67 and col. 9, lines 1-12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement bus interface conforming to a USB standard, a SCSI standard, and a fiber standard as taught by Cepulis in the system of Bell, Bell (6,170,030), and Kotha to interface with a wide range of peripheral standards.

6. Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bell (6,266,778) (herein after Bell) in view of Bell (6,170,030) (hereinafter Bell (6,170,030)), and in view of Cherukuri et al. (5,745,732) (hereinafter Cherukuri).

As to claim 21, Bell teaches a bus interface system, comprising: fist and second bus interface controllers (interface 882) (Fig. 8 and col. 6, lines 50-61 wherein bridge 810 supports multiple-bus connections) for coupling to at least one backend device (a device on the buses); a third bus interface controller (interface 834) for coupling to an internal bus of an information handling system, wherein the third bus interface controller is coupled to the first and second bus interfaces via an interface including a command queuing interface (queues 824, 828 and/or queues 852, 854) suitable for enqueuing a transaction; a command completion interface (queues 824, 828 and/or queues 852, 854) suitable for reporting transaction completion; and a data transfer interface (queues 826, 830 and/or queues 856, 858) suitable for transferring data, wherein the command queuing interface and the command completion interface are decoupled from the data transfer interface (Fig. 8). However, Bell does not explicitly disclose the command queuing interface including a first path and the command completion interface including a second

path. Bell (6,170,030) teaches separate command queue including a first path (request queues 39 and/or 41) and command completion queue including a second path (DRC queues 43 and/or 45) (Fig. 2 and col. 6 line 19 to col. 7 line 31). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement separate command queue including a first path and command completion queue including a second path as taught by Bell (6,170,030) in the system of Bell to allow the command queue and the completion queue to operate in parallel fashion (col. 7 lines 1-53) and thus improve the system's speed. However, Bell and Bell (6,170,030) do not explicitly disclose an arbiter for resolving competing demands of the first and second bus interface controllers. Cherukuri teaches arbiter (in system controller 260) for resolving competing demands between interface controllers (Figs. 2-3 and col. 3, lines 65-67, col. 4, lines 1-5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include arbiter for resolving competing demands between interface controllers as taught by Cherukuri in the system of Bell and Bell (6,170,030) to provide fairness accessing.

A to claim 22, Bell (6,170,030) further teaches command queuing and command completion have separated paths (as addressed above in claim 21).

As to claim 23, Bell further teaches multiple agents are supported (Fig. 8).

7. Claims 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bell (6,266,778) (herein after Bell) in view of Bell (6,170,030) (hereinafter Bell (6,170,030) and

Cherukuri et al. (5,745,732) (hereinafter Cherukuri), and further in view of Cepulis et al. (6,061,754) (hereinafter Cepulis).

As to claims 24, 25, the argument above for claim 23 applies. However, Bell, Bell (6,170,030), and Cherukuri do not explicitly disclose the first bus interface controller is SCSI controller, the second bus interface controller is fibre interface controller, and the third bus interface controller is one of the group consisting of a PCI interface controller and a PCI-X interface controller. Cepulis teaches bus bridge/switch interfaces conforming to a SCSI standard, a fiber standard, and a PCI standard (co. 8, lines 64-67 and col. 9, lines 1-12 and col. 1, lines 32-47). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement bus interfaces conforming to a SCSI standard, a fiber standard, and a PCI standard as taught by Cepulis in the system of Bell, Bell (6,170,030), and Cherukuri to interface with a wide range of peripheral standards.

As to claim 26, Bell further teaches commands that are processed by the bus interface system include configuration, input/output, and memory (Fig. 8 and col. 7, lines 24-30, col. 14, lines 64-67, col. 15, lines 17-29).

8. Claims 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bell (6,266,778) (herein after Bell) in view of Bell (6,170,030) (hereinafter Bell (6,170,030), Cherukuri et al. (5,745,732) (hereinafter Cherukuri), and Cepulis et al. (6,061,754) (hereinafter Cepulis), and further in view of Kotha et al. (6,067,071) (hereinafter Kotha).

As to claim 27, the argument above for claim 26 applies. However, Bell, Bell (6,170,030), Cherukuri, and Cepulis do not explicitly disclose the first and third bus interface controllers are cores. Kotha teaches core logic (chipset) (col. 1, lines 14-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the first and third bus interface controllers to be cores (integrated into a chipset) as taught by Kotha in the system of Bell, Bell (6,170,030), Cherukuri, and Cepulis to allow the circuit's functionality to be placed in smaller, lighter packages.

As to claim 28, Bell further teaches the commands that are processed are processed through at least on transfer cycle and a completion cycle that occurs after termination of the at least one transfer cycle (at least col. 1, lines 36-52).

As to claim 29, Bell further teaches a fourth bus interface controller, wherein the fourth bus interface controller is coupled to the third bus interface controller through the arbiter, wherein the arbiter resolves completing demands between the first, second, and fourth bus interface controllers (Fig. 8 and col. 6, lines 50-61 wherein bridge 810 supports multiple-bus connection interfaces).

9. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig et al. (6,449,677) (hereinafter Olarig) in view of Bell (6,266,778), and further in view of Kotha et al. (6,067,071) (hereinafter Kotha).

As to claim 30, Olarig teaches a bus interface system, comprising: a SCSI controller; a PCI-X interface controller; and an interface for coupling the SCSI controller and the PCI-X controller (PCI-X/SCSI bus interface 114) (note at least Fig. 1). However,

Olarig does not explicitly disclose the interface include a command queuing interface suitable for enqueuing a transaction; a command completion interface suitable for reporting transaction completion from the PCI interface controller to the SCSI controller; and a data transfer interface suitable for transferring data. Bell teaches an interface include a command queuing interface (queues 824, 828 and/or queues 852, 854) suitable for enqueuing a transaction; a command completion interface (queues 824, 828 and/or queues 852, 854) suitable fro reporting transaction completion from the PCI interface controller to the SCSI controller; and a data transfer interface (queues 826, 830 and/or queues 856, 858) suitable for transferring data (Fig. 8 and col. 13, lines 53-64). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the interface as taught by Bell in the system of Olarig to allow faster transaction (col. 13, lines 53-64). However, Olarig and Bell do not explicitly disclose the PCI-X interface controller being implemented as a core. Kotha teaches core logic (chipset) (col. 1, lines 14-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the PCI-X interface controller to be a core (integrated into a chipset) as taught by Kotha in the system of Bell to allow the circuit's functionality to be placed in smaller, lighter packages.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the art discloses separate request and completion queues:

US Patent 6,631,437 Callison et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 703-305-5959. The examiner can normally be reached on Mon-Thur and alternate Fri from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha Vu

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Sumati Lefkowitz

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PRIMARY EXAMINER